Listing of Claims:

1. (Original) A method comprising:

buffering a differential clock signal with a single buffer circuit for a plurality of load circuits; and

configuring the single buffer circuit to adjust to alterations in the number of load circuits receiving the differential clock signal, wherein noise immunity is increased.

2. (Original) The method of claim 1 wherein buffering further comprises buffering the differential clock signal with a differential amplifier circuit including a programmable impedance circuit and a programmable current source circuit.

3. (Original) The method of claim 2 wherein configuring the single buffer circuit further comprises adjusting an impedance level of the programmable impedance circuit and adjusting a current source level of the programmable current source circuit.

4. (Original) The method of claim 3 wherein adjusting the impedance level and adjusting the current level further comprises utilizing a plurality of control signals to selectively activate switches in the programmable impedance circuit and programmable current source circuit.

5. (Original) The method of claim 4 wherein utilizing a plurality of control signals further comprises utilizing differing logic levels of a same control signal to add, in parallel, a resistor within the programmable impedance circuit and a current source within the programmable current source circuit.

6. (Original) A circuit comprising:

a clock signal source providing a differential clock signal; and

a configurable buffer circuit for receiving the differential clock signal and providing a clock signal output for a plurality of load circuits, wherein the configurable buffer circuit achieves a constant bandwidth and voltage level for the clock signal output while adjusting to alterations in the number of load circuits coupled to the configurable buffer circuit, wherein noise immunity is increased.

7. (Original) The circuit of claim 6 wherein the configurable buffer circuit further comprises a differential amplifier circuit including a programmable output impedance circuit and a programmable current source circuit.

8. (Original) The circuit of claim 7 wherein the programmable output impedance circuit further comprises a first resistor, a plurality of second resistors, and a first plurality of switches, each switch coupling the first resistor to one of the plurality of second resistors in a parallel arrangement.

9. (Original) The circuit of claim 8 wherein the programmable current source circuit further comprises a first current source device, a plurality of second current source devices, and a second plurality of switches, each switch coupling the first current source device to one of the plurality of the second current source devices in a parallel arrangement.

10. (Original) The circuit of claim 9 further comprising control for providing control signals to each of the first and second plurality of switches to activate and deactivate each switch.

11. (Original) The circuit of claim 10 wherein the control further utilizes differing logic levels of a same control signal to control corresponding switches in the first and second plurality of switches.

12. (Original) The circuit of claim 9 wherein the first current source device and the plurality of second current source devices receive a same bias voltage.

13. (Original) A buffer circuit comprising:

a differential amplifier circuit for receiving a differential input signal, the differential amplifier circuit including a programmable impedance circuit and a programmable current source circuit to provide a constant bandwidth and voltage level for a differential output clock signal wherein the differential output clock signal is received by a variable number of load circuits.

14. (Original) The buffer circuit of claim 13 wherein the programmable impedance circuit further comprises a first resistor, a plurality of second resistors, and a first plurality of switches, each switch coupling the first resistor to one of the plurality of second resistors in a parallel arrangement.

15. (Original) The buffer circuit of claim 14 wherein the programmable current source circuit further comprises a first current source device, a plurality of second current source

devices, and a second plurality of switches, each switch coupling the first current source device to one of the plurality of the second current source devices in a parallel arrangement.

16. (Original) The buffer circuit of claim 15 further comprising control for providing control signals to each of the first and second plurality of switches to activate and deactivate each switch.

17. (Original) The buffer circuit of claim 16 wherein the control further utilizes differing logic levels of a same control signal to control corresponding switches in the first and second plurality of switches.

18. (Original) The buffer circuit of claim 15 wherein the first current source device and the plurality of second current source devices receive a same bias voltage.

19. (Previously presented) A method comprising:

buffering a differential clock signal with a single buffer circuit for a plurality of load circuits, wherein the single buffer circuit comprises a differential amplifier circuit including a programmable impedance circuit and a programmable current source circuit; and

configuring the single buffer circuit to adjust to alterations in the number of load circuits receiving the differential clock signal by adjusting an impedance level of the programmable impedance circuit and adjusting a current source level of the programmable current source circuit, wherein noise immunity is increased.

20. (Previously presented) A circuit comprising:

a clock signal source providing a differential clock signal; and

a configurable buffer circuit for receiving the differential clock signal and providing a clock signal output for a plurality of load circuits, wherein the configurable buffer circuit comprises a differential amplifier circuit including a programmable output impedance circuit and a programmable current source circuit, wherein the programmable output impedance circuit further comprises a first resistor, a plurality of second resistors, and a first plurality of switches, each switch coupling the first resistor to one of the plurality of second resistors in a parallel arrangement, and wherein the configurable buffer circuit achieves a constant bandwidth and voltage level for the clock signal output while adjusting to alterations in the number of load circuits coupled to the configurable buffer circuit, wherein noise immunity is increased.

21. (Previously presented) A buffer circuit comprising:

a differential amplifier circuit for receiving a differential input signal, the differential amplifier circuit including a programmable impedance circuit comprising a first resistor, a plurality of second resistors, and a first plurality of switches, each switch coupling the first resistor to one of the plurality of second resistors in a parallel arrangement, and a programmable current source circuit to provide a constant bandwidth and voltage level for a differential output clock signal wherein the differential output clock signal is received by a variable number of load circuits.